

100Gbps QSFP28 Active Optical Cable

NNA-100G-5M

Overview:

The NETRO's NNA-100G-5M series are active optical cables(AOC) that allows bi-directional 100Gbps transmission suitable for high performance computing (HPC) clustering and other high-throughput data network, with advantages such as high speed, high density, low latency, low power consumption and light weight.



Features:

- Quad Small Form-factor Pluggable (QSFP)
- Maximum Aggregate Data Rate 100Gbps
- EDR, FDR, QDR, DDR, SDR (Infiniband)
- 10/25/40/100G Ethernet
- Bi-directional parallel link
- BER<1e-12 From 0 to 50 degree case temp
- CDR no/off automatically
- 10/14/25/28Gb/s per lane, x4 channels
- Up to 70m (OM3)
- Up to 100m (OM4)
- Low power consumption
- Round multi-mode fiber array
- 850nm VCSEL four array
- PIN diode four array
- Hot Pluggable
- 12C management interface
- 3.3V power supply voltage
- Maximum 2W power consumption

Application:

- Low-latency and high-speed interconnections for high performance computing (HPC)
- 100G Ethernet
- Other high-throughput data transmission network

Standard:

- Compliant with IEEE 802.3ba-2010,Annex 86A for 40GBASE-SR4
- Compliant with InfiniBand QDR,DDR,SDR
- Compliant with QSFP MSA(SFF-8436)
- ROHS Compliant: lead-free

Performance Specifications:

Absolute Maximum Ratings

These values represent the damage threshold of the module. Stress in excess of any of the individual Absolute Maximum Ratings can cause immediate catastrophic damage to the module even if all other parameters are within Recommended Operating Conditions.

Absolute maximum ratings:

Parameter	Conditions	Min	Max	Units
Power supply voltage at 3.3V		-0.5	3.75	V
Voltage on I/O pads		-0.5	VDD+0.5	V
Differential Input Swing			1.5	Vpp
Storage temperature	Non-condensing	-40	85	Celsius
Powered case temperature range	Non-condensing	-5	70	Celsius
Relative Humidity		5	85	%
Static discharge voltage on high speed pins	Human body model		500	V
Static discharge voltage on other pins	Human body model		2000	V
Air discharge to QSFP case	EN61000-4-2 Criterion B Test		15	kV
Contact discharge to QSFP case	EN61000-4-2 Criterion B Test		8	kV

Recommended Operating Conditions:

Parameter	Conditions	Min	Typ.	Max	Units
Data rate per lane	8B/10B Coding, 64B/66B Coding	1	10.3125	10.5	Gbps
3.3V Supply Voltage		3.13	3.3	3.47	V
Power supply noise including ripples	1kHz to frequency of operation mersured at VCC_HOST			50	mVpp
Case temperature		0	35	70	Celsius

Transmitter Specifications (Electrical):

Symbol	Parameter	Specification value.	Unit	Note
X1,X2	Eye mask parameter,time	0.11,0.31	UI	At FDR,EDR rates See Figure 1
Y1,Y2	Eye mask parameter,voltage	95,350	mV	
X	Eye mask parameter,time	0.15	UI	At SDR,DDR rates See Figure 2
Y1,Y2	Eye mask parameter,voltage	250,600	mV	

Symbol	Parameter	Min	Typical	Max.	Unit	Notes
DDPWS	Data Dependent pulse Width Shrinkage			0.11	UI	
J2	J2 jitter tolerance			0.19	UI	With TX CDR bypassed (i.e., disabled)
				0.44	UI	With TX CDR enabled
J9	J9 jitter tolerance			0.34	UI	With TX CDR bypassed (i.e., disabled)
				0.69	UI	With TX CDR enabled
S_{DD11}	Differential input return loss				dB	See Equation 1 & Figure 3
S_{CC11}	Common mode input return loss			-2	dB	
S_{DC11}	Common mode to differential reflection				dB	See Equation 2 & Figure 4
	Skew between channels			50	ps	Skew resulted from module.

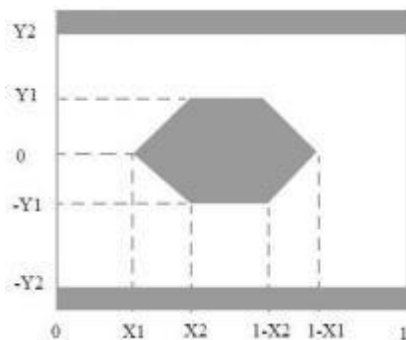


Figure 1

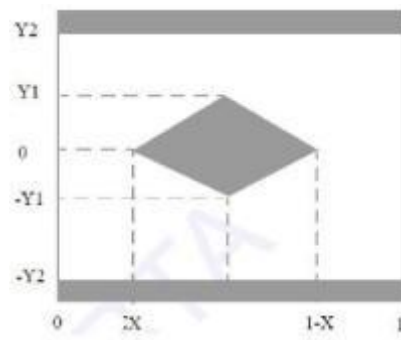


Figure 2

Receiver Specification (Electrical)

Symbol	Parameter	Specification value.	Unit	Notes
X	Eye mask parameter,time	0.3	UI	Hit ratio=5E-5
Y1,Y2	Eye mask parameter,voltage range 0	50,225	mV	
	range 1	100,350		
	range 2	150,450		

Symbol	Parameter	Min	Typical	Max.	Unit	Notes
	Differential Output swing(p-p)		320 (range 0)		mV	Amplitude code 0000 Amplitude code is set at page03 byte 238-239, 4 bits for each channel. See details in the section "Memory Map"
			420 (range 1)		mV	Factory default Amplitude code 0001
			TBD (range 2)		mV	Amplitude code 0010 & 0011
				50	mV	Squelched state
S _{DD22}	Differential output return loss				dB	See Equation 1 & Figure 3
S _{CC22}	Common mode output return loss			-2	dB	
S _{DC22}	Common mode to differential reflection				dB	See Equation 2 & Figure 4
J2	J2 jitter			0.44	UI	
J9	J9 jitter			0.69	UI	
	Skew between channels			50	ps	Skew resulted from module.

Data Rate Specification:

Symbol	Parameter	Min	Typical	Max.	Unit	Notes
BR	Bit Rate per Lane	10	25.781	28	Gbps	Lower BER performance at 28Gbps
BER	Bit Error Rate			10^{-12}		1.2.3

1. Bit Error Rate is tested with PRBS 231-1 pattern at 25.781Gbit/s.
2. 100G QSFP28 AOC requires an electrical connector compliant with SFF-8662 or SFF-8672 which is used on the host board in order to guarantee its electrical interface specification.
3. Subject to operating condition. Temperature range tested: 25°C ~ < 60°C.

Equation1:
$$S_{DDxx} \leq \begin{cases} -15 + 1.5\sqrt{f} & 0.05 \leq f < 4.6 \\ -10.66 + 14 * \log_{10}(f/5.5) & 4.6 \leq f < 26 \end{cases} \quad f \text{ is frequency in GHz}$$

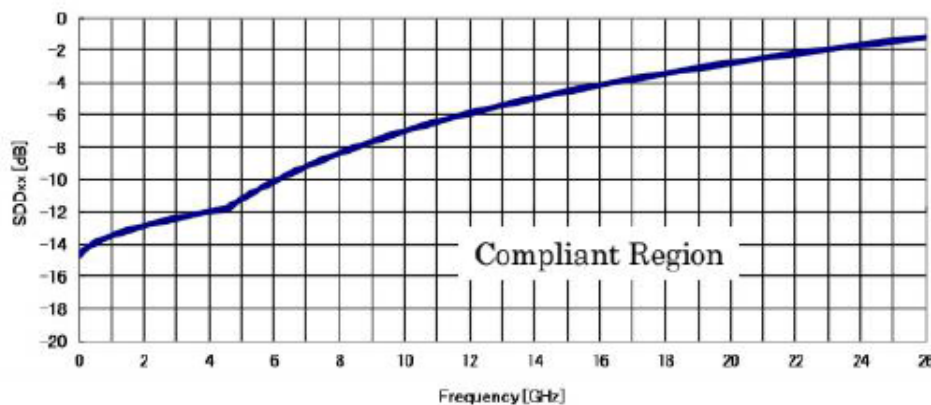


Figure 3: Limits on S_{DD11} and S_{DD22} vs. Frequency for EDR

Equation2:
$$S_{DCxx} \leq \text{MIN}\left(-16 + \frac{2}{3}f, 0\right) \quad 0.05 \leq f < 26 \quad f \text{ is frequency in GHz}$$

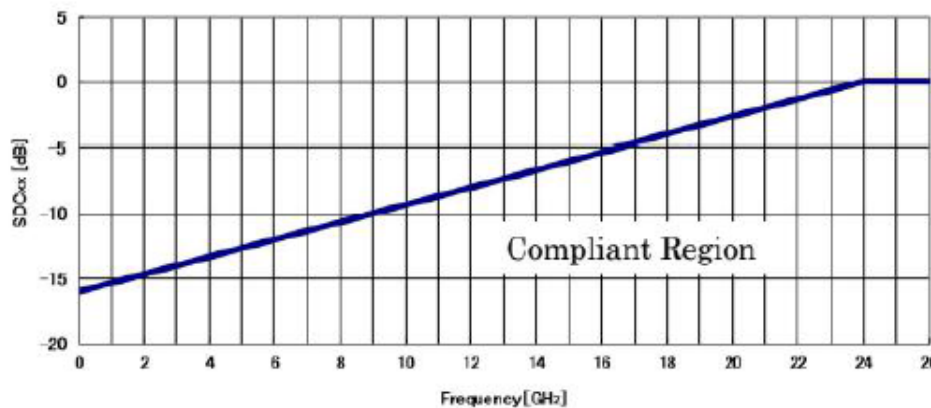
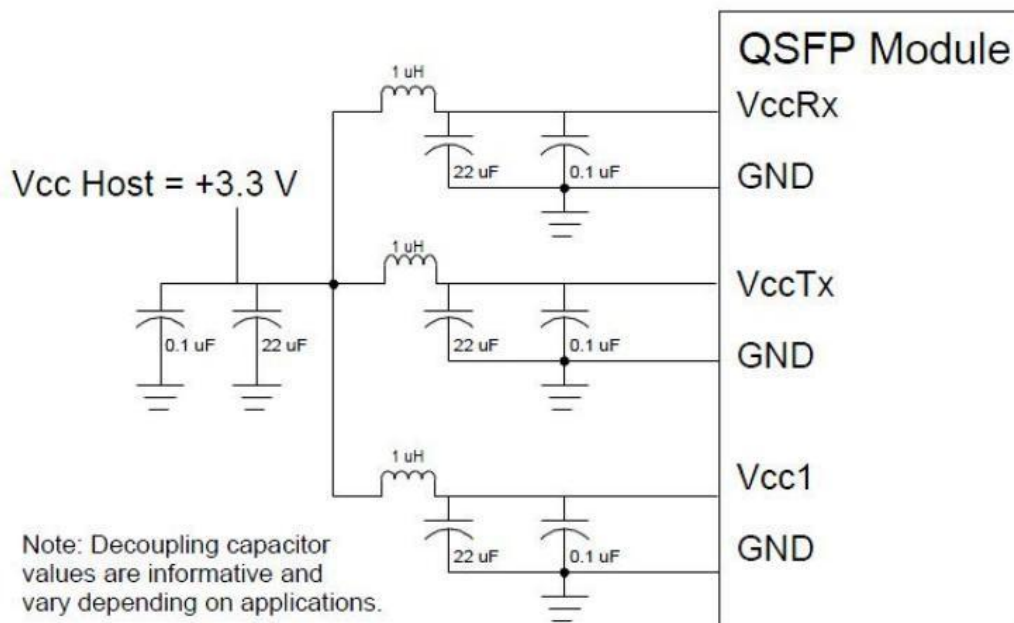


Figure 4: Limits on S_{DC11} and S_{DC22} vs. Frequency for EDR

Low Speed Electrical Specification

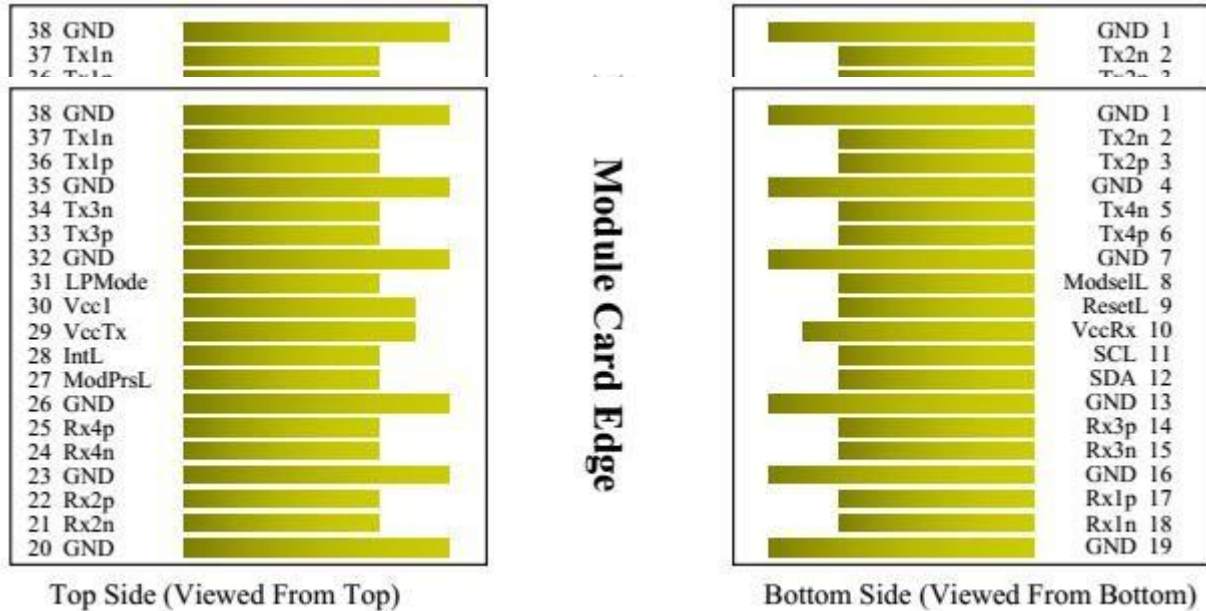
Parameter	Symbol	Min	Max.	Unit	Notes
Reset, ModSel, LPMMode	VIL	-0.3	0.8	V	Lower BER performance at 28Gbps
	VIH	2	VCC+0.3	V	
ModPral					Internally terminated to GND
IntL	VOL	0	0.4	V	IOL=2mA
	VOH	VCC-0.5	VCC+0.3	V	
SCL, SDA	VOL	0	0.4	V	IOL(max)=3mA
	VOH	VCC-0.5	VCC+0.3	V	
	VIL	-0.3	VCC*0.3	V	
	VIH	VCC*0.7	VCC+0.5	V	
Capacitance for SCL and SDA I/O Pin	Ci		14	pF	
Total bus capacitance load for SCL and SDA	Cb		100	pF	3.0kohm Pullup resistor, max
			200	pF	1.6kohm Pullup resistor, max

Recommended QSFP Host Board Power Supply Filtering



Recommended QSFP Host Board Power Supply Filtering

PIN Definitions:



PIN Definitions:

Pin number	Logic	Symbol	Signal	Description
1		GND	Signal Ground	Ground
2	CML-I	Tx2n	Tx2n	Transmitter Inverted Date Input.AC coupled
3	CML-I	Tx2p	Tx2p	Transmitter Non_Inverted Date Input.AC coupled
4		GND	Signal Ground	Ground
5	CML-I	Tx4n	Tx4n	Transmitter Inverted Date Input.AC coupled
6	CML-I	Tx4p	Tx4p	Transmitter Non_Inverted Date Input.AC coupled
7		GND	Signal Ground	Ground
8	LVTTL-I	ModSelL	ModSelL	Module Select pin.Selected when held low by the host.
9	LVTTL-I	ResetL	LPMode_Reset	Module Reset.A"low" pulse induces a reset on the module.
10		Vcc Rx	Vcc Rx	+3.3V Power Supply Receiver
11	LVC MOS-I/O	SCL	SCL	2-wire serial interface
12	LVC MOS-I/O	SDA	SDA	
13		GND	Signal Ground	Ground
14	CML-O	Rx3p	Rx3p	Receiver Non_Inverted Date Input.AC coupled
15	CML-O	Rx3n	Rx3n	Receiver Inverted Date Input.AC coupled
16		GND	Signal Ground	Ground
17	CML-O	Rx1p	Rx1p	Receiver Non_Inverted Date Input.AC coupled
18	CML-O	Rx1n	Rx1n	Receiver Inverted Date Input.AC coupled
19		GND	Signal Ground	Ground
20		GND	Signal Ground	Ground
21	CML-O	Rx2n	Rx2n	Receiver Inverted Date Input.AC coupled
22	CML-O	Rx2p	Rx2p	Receiver Non_Inverted Date Input.AC coupled
23		GND	Signal Ground	Ground
24	CML-O	Rx4n	Rx4n	Receiver Inverted Date Input.AC coupled
25	CML-O	Rx4p	Rx4p	Receiver Non_Inverted Date Input.AC coupled

26		GND	Signal Ground	Ground
27	LVTTTL-O	ModPrsL	ModPrsL	Module Present pin. Internally grounded inside the module.
28	LVTTTL-O	IntL	IntL	Interrupt by the QSFP module. "Low" indicates an Alarm/Warning.
29		Vcc Tx	Vcc Tx	+3.3V Power Supply Transmitter
30		Vccl	Vccl	+3.3V Power Supply
31	LVTTTL-I	LPMode	LPMode	Low Power Mode
32		GND	Signal Ground	Ground
33	CML-I	Tx3p	Tx3p	Transmitter Non_Inverted Date Input.AC coupled
34	CML-I	Tx3n	Tx3n	Transmitter Inverted Date Input.AC coupled
35		GND	Signal Ground	Ground
36	CML-I	Tx1p	Tx1p	Transmitter Non_Inverted Date Input.AC coupled
37	CML-I	Tx1n	Tx1n	Transmitter Inverted Date Input.AC coupled
38		GND	Signal Ground	Ground
Housing			Chassis Ground	

